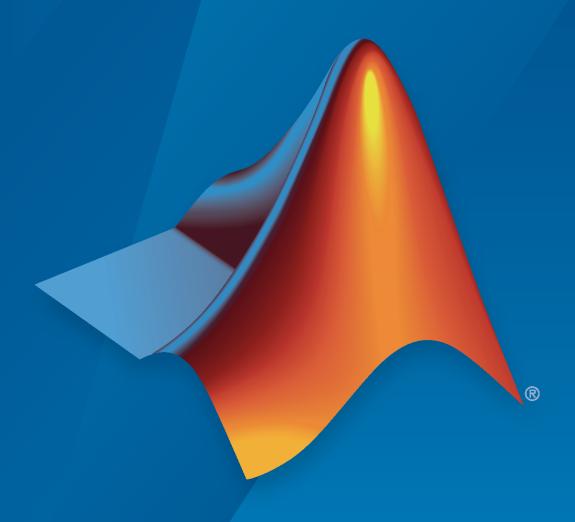
### Simulink<sup>®</sup>

Modeling Guidelines for Code Generation



# MATLAB&SIMULINK®



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Modeling Guidelines for Code Generation

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### **Revision History**

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April 2011	Online only	Revised for Version 1.1 (Release 2011a)
September 2011	Online only	Revised for Version 1.2 (Release 2011b)
March 2012	Online only	Revised for Version 1.3 (Release 2012a)
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September 2013	Online only	Revised for Version 1.6 (Release 2013b)
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### Introduction

- "Motivation" on page 1-2
- ullet "Guideline Template" on page 1-3

### **Motivation**

MathWorks intends the guidelines for engineers developing models and generating code for embedded systems using Model-Based Design with MathWorks products. The guidelines provide recommendations for model settings, block usage, and block parameters that impact simulation behavior or code generated by the Embedded Coder® product.

The guidelines do not address model style or development processes. For more information about creating models in a way that improves consistency, clarity, and readability, see the "MAB Modeling Guidelines". Development process guidance and additional information for specific standards is available with the IEC Certification Kit (for ISO 26262 and IEC 61508) and DO Qualification Kit (for DO-178) products.

**Disclaimer** While adhering to the recommendations in the guidelines will reduce the risk that an error is introduced during development and not be detected, it is not a guarantee that the system being developed will be safe. Conversely, if some of the recommendations in the guidelines are not followed, it does not mean that the system being developed will be unsafe.

### **Guideline Template**

Guideline descriptions are documented, using the following template. Companies that want to create additional guidelines are encouraged to use the same template.

**ID: Title** XX nnnn: Title of the guideline (unique, short)

**Description** Description of the guideline

**Prerequisites** Links to guidelines that are prerequisites to this guideline (ID: Title)

**Notes** Notes for using the guideline

**Rationale** Rationale for providing the guideline

Model Title of and link to the corresponding Model Advisor check, if a check exists

Advisor Check

**References** References to standards that apply to guideline

See Also Links to additional information
Last Changed Version number of last change

**Examples** Guideline examples

### **Block Considerations**

- "cgsl\_0101: Zero-based indexing" on page 2-2
- "cgsl 0102: Evenly spaced breakpoints in lookup tables" on page 2-3
- "cgsl 0103: Precalculated signals and parameters" on page 2-4
- "cgsl\_0104: Modeling global shared memory using data stores" on page 2-7
- "cgsl\_0105: Modeling local shared memory using data stores" on page 2-10

### cgsl\_0101: Zero-based indexing

ID: Title	cgsl_0101: Zero-based indexing			
Description	Use zero-based indexing for blocks that require indexing. To set up zero-based indexing, do one of the following:			
	A For the Index Vector block parameter <b>Data port order</b> , select Zero-based contiguous.			
	B Set block parameter <b>Index mode</b> to Zero-based for the following blocks:			
	Assignment			
	Selector			
	For Iterator			
	Find Nonzero Elements			
Notes	The C language uses zero-based indexing.			
Rationale	A, B Use zero-based indexing for compatibility with integrated C code.			
	A, B Results in more efficient C code execution. One-based indexing requires a subtraction operation in generated code.			
See Also	"hisl_0021: Consistent vector indexing method"			
Last Changed	R2011b			
	1 IndexSel_Zero 2 3 ZeroIndexSerray			
	Recommended			
	void ZeroIndex(void)			
	<pre>{    Y.Out5 = 3.0 * ZeroIndexArray[IndexSel_Zero]; }</pre>			
	1 IndexSel_One 63 1			
	Not Recommended			
	void OneIndex(void)			
	<pre>{    Y.Out1 = OneIndexArray[IndexSel_One - 1] * 6.3; }</pre>			

### cgsl\_0102: Evenly spaced breakpoints in lookup tables

ID: Title	cgsl_0102: Evenly spaced breakpoints in lookup tables				
Description	When you use Lookup Table and Prelookup blocks,				
	A	With non-fixed-point data types, use evenly spaced data breakpoints for the input axis			
	В	With <i>fixed-point data types</i> , use power of two spaced breakpoints for the input axis			
Notes	Evenly spaced breakpoints can prevent generated code from including division operations, resulting in faster execution.				
Rationale	A Improve ROM usage and execution speed.				
	В	Improve execution speed.			
		When compared to unevenly spaced data, power-of-two data can			
		Increase data RAM usage if you require a finer step size			
		Reduce accuracy if you use a coarser step size			
		Compared to an evenly spaced data set, there should be minimal cost in memory or accuracy.			
Model Advisor Checks	By Product > Embedded Coder > Identify questionable fixed-point operations				
	For check details, see "Identify questionable fixed-point operations" (Embedded Coder).				
See Also	"Formulation of Evenly Spaced Breakpoints"				
Last Changed	R2010b				

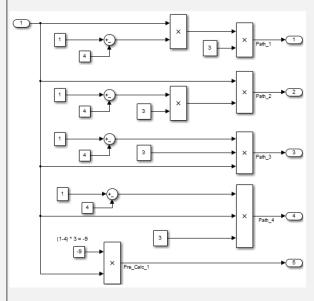
### cgsl\_0103: Precalculated signals and parameters

ID: Title	cgsl_0103: Precalculated signals and parameters		
Description	Precalcu following	llate invariant parameters and signals by doing one of the g:	
	A	Manually precalculate the values	
	В	Set these configuration parameters:	
		Set <b>Default parameter behavior</b> to Inlined	
		Select Inline invariant signals	
Notes	Precalculating variables can reduce local and global memory usage and improve execution speed. If you set <b>Default parameter behavior</b> to Inlined and enable <b>Inline invariant signals</b> , the code generator minimizes the number of run-time calculations by maximizing the number calculations completed before run time. In some cases, this can lead to a reduction in the number of parameters stored. However, the algorithms the code generator uses have limitations. In some cases, the code is more compact if you calculate the values outside of the Simulink environment. This can improve model efficiency, but can reduce model readability.		
Rationale	А, В	Precalculate data, outside of the Simulink environment, to reduce memory requirements of a system and improve run-time execution.	
Last Changed	R2012b		

### ID: Title cgsl\_0103: Precalculated signals and parameters

Examples

In the following model, the four paths are mathematically equivalent. However, due to algorithm limitations, the number of run-time calculations for the paths differs.



```
Path_1 = InputSignal * -3.0 * 3.0;
```

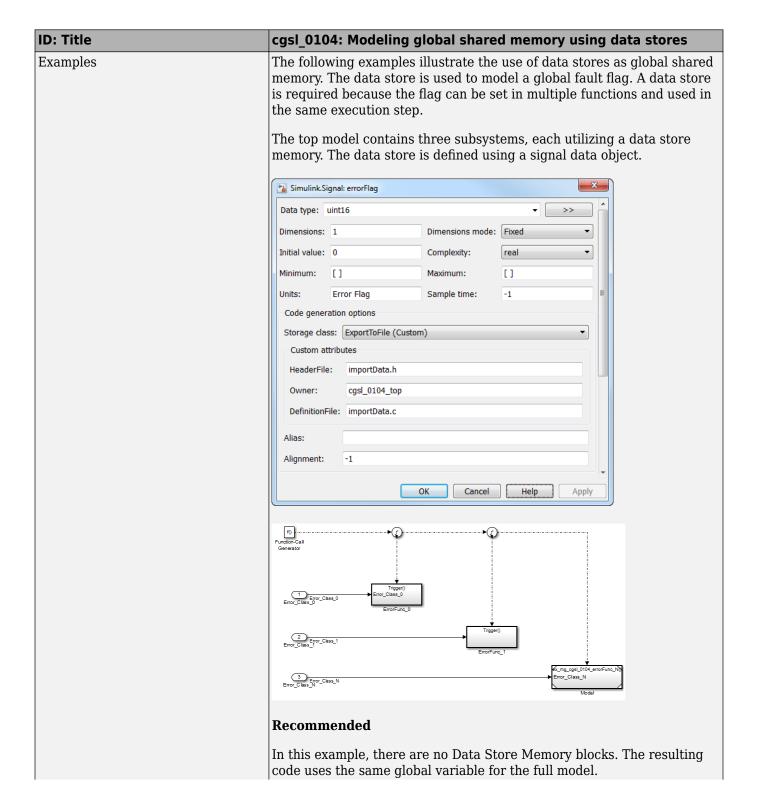
To maximize automatic precalculation, add signals at the end of the set of equations.

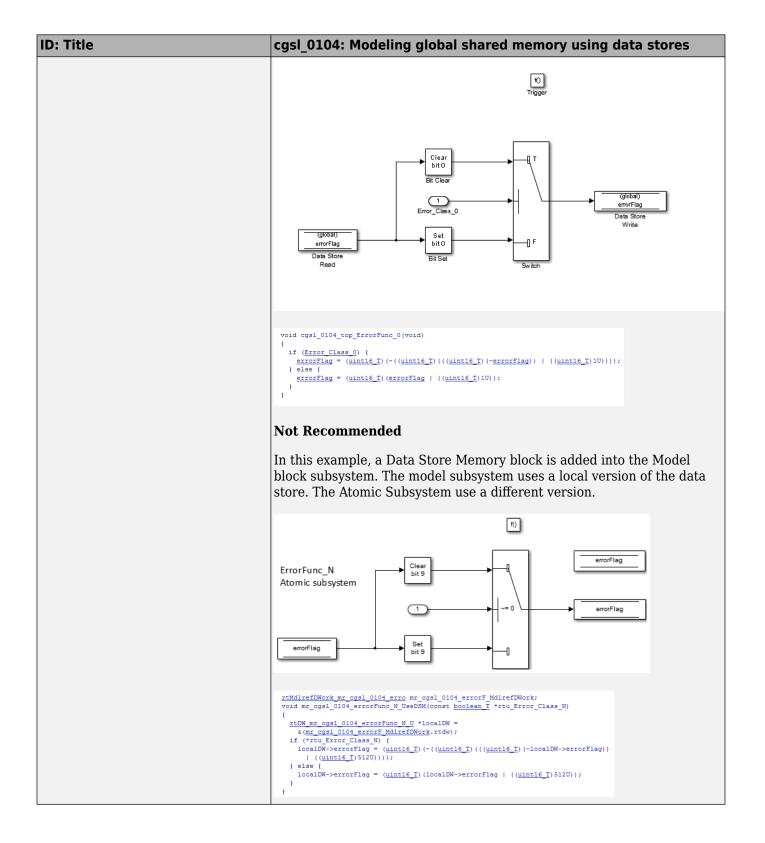
Inlining data reduces the ability to tune model parameters. You should define parameters that require calibration to allow calibration. For more

ID: Title	cgsl_0103: Precalculated signals and parameters	
	information, see "Create Tunable Calibration Parameter in the	
	Generated Code" (Simulink Coder).	

### cgsl\_0104: Modeling global shared memory using data stores

ID: Title	cgsl_0	104: Modeling global shared memory using data stores		
Description	When u	using data store blocks to model shared memory across multiple ::		
	A	Set configuration parameters <b>Duplicate data store names</b> to error for models in the hierarchy.		
	В	Define the data store using a Simulink Signal or MPT Signal object.		
	С	Do not use Data Store Memory blocks in the model.		
Notes	If multiple Data Store blocks use the same data store name within a model, then Simulink interprets each instance of the data store as having a unique local scope.			
	Use <b>Duplicate data store names</b> to help detect unintended identifier reuse. For models intentionally using local data stores, set the diagnostic to warning. Verify that only intentional data stores are included.  Merge blocks, used in conjunction with subsystems operating in a mutually exclusive manor, provide a second method of modeling global data across multiple models.			
Rationale	A, B, C	Promotes a modeling pattern where a single consistent data store is used across models and a single global instance is created in the generated code.		
See Also	• "his	sl_0013: Usage of data store blocks"		
	"hisl_0015: Usage of Merge blocks"			
	• "cgsl_0302: Diagnostic settings for multirate and multitasking models" on page 4-3			
	"cgsl_0105: Modeling local shared memory using data stores" on page 2-10			
Last Changed	R20111	R2011b		





### cgsl\_0105: Modeling local shared memory using data stores

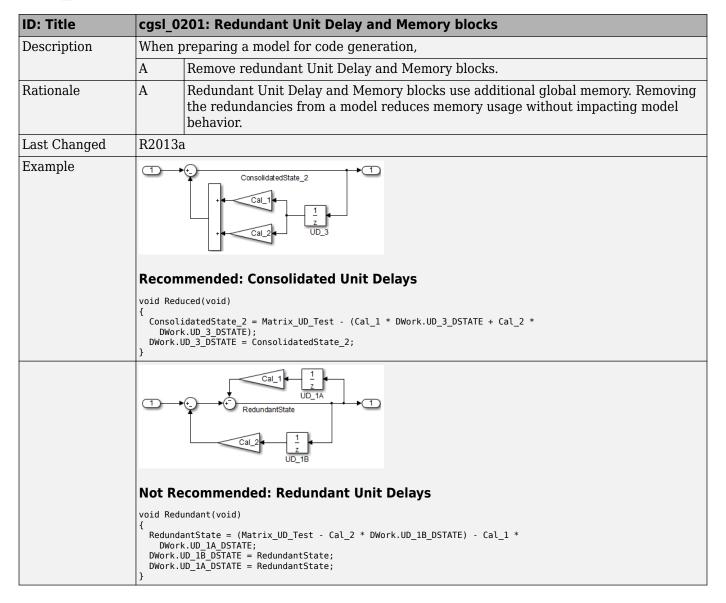
ID: Title	cgsl_0105: Modeling local shared memory using data stores			
Description	When using data store blocks as local shared memory:			
	A Explicitly create the data store using a Data Store Memory block.			
	В	Clear block parameter <b>Data store name must resolve to Simulink signal object</b> .		
	С	Consider following a naming convention for local Data Store Memory blocks.		
Notes	Use configuration parameter <b>Duplicate data store names</b> to help detect unintended identifier reuse. For models intentionally using local data stores, set the diagnostic to warning. Verify that only intentional data stores are included.  Data store blocks are realized as global memory in the generated code. If they are not assigned a specific storage class, they are included in the DWork structure. In the model, the data store is scoped to the defining subsystem and below. In the generated code, the data store has file			
Rationale	scope. A, B	Data store block is treated as a local instance of the data store		
	С	Provides graphical feedback that the data store is local		
See Also	"cgsl_0104: Modeling global shared memory using data stores" on page 2-7			
	• "cgsl_0302: Diagnostic settings for multirate and multitasking models" on page 4-3			
	"hisl_0013: Usage of data store blocks"			
Last Changed	R2011b			

### **ID: Title** cgsl\_0105: Modeling local shared memory using data stores **Examples** In some instances, such as a library function, reuse of a local data store is required. In this example, the local data store is defined in two subsystems. The instance of localFlag is in scope within the subsystem LocalDataStore\_1 and its subsystems. /\* Block signals and states (auto storage) for system '<Root>' \*/ typedef struct { real T localFlag; real T localFlag\_k; /\* '<S2>/DSM Loc 2' \*/ /\* '<S1>/DSM Loc 1' \*/ } D\_Work\_cgsl\_0105; In the generated code, the data stores are part of the global DWork structure for the model. Embedded Coder automatically assigns them unique names during the code generation process.

### **Modeling Pattern Considerations**

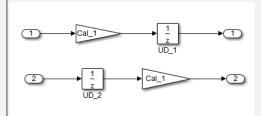
- "cgsl 0201: Redundant Unit Delay and Memory blocks" on page 3-2
- "cgsl 0202: Usage of For, While, and For Each subsystems with vector signals" on page 3-6
- "cgsl\_0204: Vector and bus signals crossing into atomic subsystems or Model blocks" on page 3-7
- "cgsl\_0205: Signal handling for multirate models" on page 3-12
- "cgsl 0206: Data integrity and determinism in multitasking models" on page 3-14

### cgsl\_0201: Redundant Unit Delay and Memory blocks



### ID: Title cgsl\_0201: Redundant Unit Delay and Memory blocks

Unit Delay and Memory blocks exhibit commutative and distributive algebraic properties. When the blocks are part of an equation with one driving signal, you can move the Unit Delay and Memory blocks to a new position in the equation without changing the result.



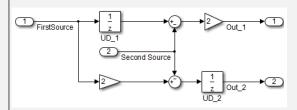
For the top path in the preceding example, the equations for the blocks are:

- $1 \quad \text{Out}_1(t) = \text{UD}_1(t)$
- 2 UD\_1(t) = In\_1(t-1) \* Cal\_1

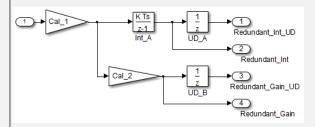
For the bottom path, the equations are:

- 1 Out 2(t) = UD 2(t) \* Cal 1
- 2 UD 2(t) = In 2(t-1)

In contrast, if you add a secondary signal to the equations, the location of the Unit Delay block impacts the result. As the following example shows, the location of the Unit Delay block impacts the results due to the skewing of the time sample between the top and bottom paths.



In cases with a single source and multiple destinations, the comparison is more complex. For example, in the following model, you can refactor the two Unit Delay blocks into a single unit delay.



# ID: Title cgsl\_0201: Redundant Unit Delay and Memory blocks | The call | Th

rtb\_Gain4 = Cal\_1 \* Redundant;
Y.Redundant\_Gain = Cal\_2 \* rtb\_Gain4;
Y.Redundant\_Int = DWork.Int\_A;
Y.Redundant\_Int\_UD = DWork.UD\_A;
Y.Redundant\_Gain\_UD = DWork.UD\_B;
DWork.Int\_A = 0.01 \* rtb\_Gain4 + DWork.Int\_A;
DWork.UD\_A = Y.Redundant\_Int;
DWork.UD\_B = Y.Redundant\_Gain;
}
{
 real\_T rtb\_Gain1;
 real\_T rtb UD C;

Y.Reduced\_Gain\_UD = Cal\_2 \* DWork.UD\_C;
Y.Reduced Gain = Cal 2 \* rtb Gain1;

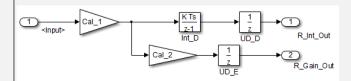
rtb\_Gain1 = Cal\_1 \* Reduced; rtb UD C = DWork.UD C;

Y.Reduced\_Int = DWork.Int\_B;
Y.Reduced\_Int\_UD = DWork.Int\_C;

DWork.UD C = rtb Gain1;

In this case, the original model is more efficient. In the first code example, there are three global variables, two from the Unit Delay blocks (DWork.UD\_A and DWork.UD\_B) and one from the discrete time integrator (DWork.Int\_A). The second code example shows a reduction to one global variable generated by the unit delays (Dwork.UD\_C), but there are two global variables due to the redundant Discrete Time Integrator blocks (DWork.Int\_B and DWork.Int\_C). The Discrete Time Integrator block path introduces an additional local variable (rtb\_UD\_C) and two additional computations.

By contrast, the refactored model (second) below is more efficient.



```
ID: Title
                   cgsl 0201: Redundant Unit Delay and Memory blocks
                                                  Cal 2
                                                                    Gain_Out
                    {
                      real_T rtb_Gain4_f:
real_T rtb_Int_D;
rtb_Gain4_f = Cal_1 * U.Input;
                      rtb_Int_D = DWork.Int_D;
                      Y.R_Int_Out = DWork.UD_D;
Y.R_Gain_Out = DWork.UD_E;
                      DWork.Int_D = 0.01 * rtb_Gain4_f + DWork.Int_D;
                      DWork.UD_D = rtb_Int_D;
                      DWork.UD_E = Cal_2 * rtb_Gain4_f;
                    {
                      real_T rtb_UD_F;
                      rtb_UD_F = DWork.UD_F;
                      Y.Gain_Out = Cal_2 * DWork.UD_F;
                      Y.Int_Out = DWork.Int_E;
                      DWork.UD_F = Cal_1 * \overline{U}.Input;
                      DWork.Int_E = 0.\overline{0}1 * rtb_UD_F + DWork.Int_E;
                   The code for the refactored model is more efficient because the branches from the root
                   signal do not have a redundant unit delay.
```

### cgsl\_0202: Usage of For, While, and For Each subsystems with vector signals

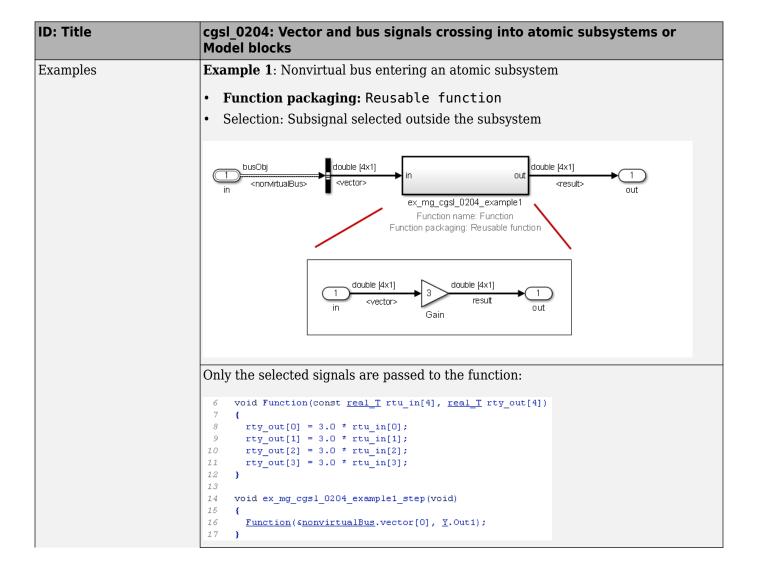
ID: Title	cgsl_0202: Usage of For, While, and For Each subsystems with vector signals			
Description	When developing a model for code generation,			
	A Use For, While, and For Each subsystems for calculations that require iterative behavior or operate on a subset (frame) of data.			
	B Avoid using For, While, or For Each subsystems for basic vector operations.			
Rationale	A, B Avoid redundant loops.			
See Also	"Loop unrolling threshold" (Simulink Coder) in the Simulink documentation			
Last Changed	R2010b			
Examples	The recommended method for preceding calculation is to place the Gain block outside the For Subsystem. If the calculations are required as part of a larger algorithm, you can avoid the nesting of for loops by using Index Vector and Assignment blocks.			
	<pre>Recommended  for (sl_iter = 0; sl_iter &lt; 10; sl_iter++) {    RecommendedOut[sl_iter] = 2.3 * vectorInput[sl_iter]; }</pre>			
	A common mistake is to embed basic vector operations in a For, While, or For Each subsystem. The following example includes a simple vector gain inside a For subsystem, which results in unnecessary nested for loops.			
	Fog. N-1 int32   Iterator N-1   Int32   Terminator			
	Not Recommended			
	<pre>for (s1_iter = 0; s1_iter &lt; 10; s1_iter++) {   for (i = 0; i &lt; 10; i++) {     NotRecommendedOut[i] = 2.3 * vectorInput[i];   } }</pre>			

# cgsl\_0204: Vector and bus signals crossing into atomic subsystems or Model blocks

ID: Title		cgsl_0204: Vector and bus signals crossing into atomic subsystems or Model blocks			
Description	When working with vector or bus signals and some of the signal elements are in an atomic subsystem or a referenced model, use the following information to determine how to select signal elements to minimize memory usage.				
	A	Bus or vector entering an atomic subsystem:			
		Function packaging: Non-reusable function Function interface: void void			
			Signals selected outside subsystem results in	Signal selected inside subsystem results in	
		Virtual Bus	No data copies.	No data copies.	
		Nonvirtual Bus	No data copies.	No data copies.	
		Vector	A copy of the selected signals in global block I/O structure that is used in the function.	No data copies.	
		Function packaging: Non-reusable function  Function interface: Allow arguments (Optimized)			
			Signals selected outside subsystem results in	Signal selected inside subsystem results in	
		Virtual Bus	No data copies. Only the selected signals are passed to the function.	No data copies. Only the selected signals are passed to the function.	
		Nonvirtual Bus	No data copies. Only the selected signals are passed to the function.	No data copies. The whole bus is passed to the function.	
		Vector	A copy of the selected signals in a local variable that is passed to the function.	No data copies. The whole vector is passed to the function.	

cgsl_0204: Vector and bus Model blocks	cgsl_0204: Vector and bus signals crossing into atomic subsystems or Model blocks				
Function packagi	ng: Reusable function				
	Signals selected outside subsystem results in	Signal selected inside the subsystem results in			
Virtual Bus	No data copies. Only the selected signals are passed to the function.	No data copies. Only the selected signals are passed to the function.			
Nonvirtual Bus	No data copies. Only the selected signals are passed to the function. See example 1.	No data copies. The whole bus is passed to the function.			
Vector	A copy of the selected signals in a local variable that is passed to the function.	No data copies. The whole vector is passed to the function.			
	Function packagi  Virtual Bus  Nonvirtual Bus	Function packaging: Reusable function  Signals selected outside subsystem results in  Virtual Bus  No data copies. Only the selected signals are passed to the function.  Nonvirtual Bus  No data copies. Only the selected signals are passed to the function. See example 1.  Vector  A copy of the selected signals in a local variable that is passed			

ID: Title	cgsl_0204: Vector and bus signals crossing into atomic subsystems or Model blocks			
	В	Bus or vector entering a Model block:		
			Signals selected outside Model block results in	Signal selected inside Model block results in
		Virtual Bus	No data copies. Only selected signals are passed to the function.	If Inport block parameter <b>Output as</b> nonvirtual bus is selected, then there are no data copies. Only the selected signals are passed to the function.
				If Inport block parameter <b>Output as nonvirtual bus</b> is cleared, then a copy of the whole bus is passed to the function.
		Nonvirtual Bus	No data copies. Only the selected signals are passed to the function.	If Inport block parameter <b>Output as</b> nonvirtual bus is selected, then there are no data copies. Only the selected signals are passed to the function.
				If Inport block parameter <b>Output as nonvirtual bus</b> is cleared, then a copy of the whole bus is passed to the function. See example 2.
		Vector	A copy of the selected signals in a local variable that is passed to the function.	No data copies. The whole vector is passed to the function.
Notes	Depending on Embedded Coder settings (e.g. optimizations), predecessor blocks and signal storage classes, actual results might differ from the tables.      Wirtual busses do not support global data.			
	<ul> <li>Virtual busses do not support global data.</li> <li>If the subsystem is set to Inline, data copies do not occur.</li> </ul>			
Rationale	A, B	Minimize RAM, ROM, ar	<u>_</u>	
Last Changed	R2016a			



### **ID: Title** cgsl 0204: Vector and bus signals crossing into atomic subsystems or Model blocks Example 2: Nonvirtual bus entering a model block Total number of instances allowed per top model: Multiple Selection: Subsignal selected inside the referenced model ex\_mg\_cgsl\_0204\_example2ref double [4x1] husOhi result <nonvirtualBus> out ex\_mg\_cgsl\_0204\_example2ref double [4x1] busObi double [4x1] 3 nonvirtualBus <vector> result out Gain There are no data copies in the code for the main model. The whole bus is passed to the model reference function. void ex\_mg\_cgsl\_0204\_example2\_step(void) ex\_mg\_cgsl\_0204\_example2ref(&ex\_mg\_cgsl\_0204\_example2\_U.nonvirtualBus, &ex\_mg\_cgsl\_0204\_example2\_U.out1[0]); 8 Code for the model reference function: void ex\_mg\_cgsl\_0204\_example2ref(const <u>bus0bj</u> \*rtu\_in, <u>real\_T</u> rty\_out[4]) 5 6 rty\_out[0] = 3.0 \* rtu\_in->vector[0]; rty\_out[1] = 3.0 \* rtu\_in->vector[1]; rty\_out[2] = 3.0 \* rtu\_in->vector[2]; rty\_out[3] = 3.0 \* rtu\_in->vector[3]; 10

### cgsl\_0205: Signal handling for multirate models

ID: Title	cgsl_0205: Signal handling for multirate models			
Description	For multirate models, handle the change in operation rate in one of two ways:			
	A	At the destination block, Insert a Rate Transition.		
	В	Set configuration parameter <b>Automatically handle rate transition for data transfer</b> to Always or Whenever possible.		
Rationale	A,B	Following this guideline supports the handling of data operating at different rates.		
Note	Setting <b>Automatically handle rate transition for data transfer</b> to Whenever possible requires you to insert a Rate Transition block in locations indicated be Simulink.			
	Setting <b>Automatically handle rate transition for data transfer</b> to Always allows Simulink to automatically handle rate transitions by inserting a Rate Transition block. The following exceptions apply:			
	<ul> <li>The insertion of a Rate Transition block requires rewiring the block diagram.</li> <li>Multiple Rate Transition blocks are required:</li> </ul>			
	• 5	The blocks' sample times are not integer multiples of each other		
	• 7	The blocks use different sample time offsets		
	One of the rates is asynchronous			
	An inserted Rate Transition block can have multiple valid configurations.			
	For these cases, manually insert a Rate Transition block or blocks.			
	MathWorks does not recommend using Unit Delay and Zero Order Hold blocks for handling rate transitions.			
Last Changed	R2011a	a a constant of the constant o		

# Examples Not Recommended: In this example, the Rate Transition block is inserted at the source, not at the destination of the signal. The model fails to update because the two destination blocks (Gain and Sum) run at different rates. To fix this error, insert Rate Transition blocks at the signal destinations and remove Rate Transition blocks from the signal sources. Failure to remove the Rate Transition blocks is a common modeling pattern that might result in errors and inefficient code. Recommended: In this example, the rate transition is inserted at the destination of the signal.

### cgsl\_0206: Data integrity and determinism in multitasking models

ID: Title	cgsl_0	206: Data integrity and determinism in multitasking models			
Description		For multitasking models that are deployed with a preemptive (interruptible) operating system, protect the integrity of selected signals by doing one of the following:			
	A	Select the Rate Transition block parameter <b>Ensure data integrity during</b> data transfer .			
	В	For Inport blocks in Function Called subsystems, select the block parameter Latch input for feedback signals of function-call subsystem outputs.			
	To pro	To protect selected signal determinism, do one of the following:			
	С	Select the Rate Transition block parameter <b>Ensure deterministic data</b> transfer (maximum delay).			
	D	• Select the configuration parameter <b>Automatically handle rate transition for data transfer</b> .			
		• Set configuration parameter <b>Deterministic data transfer</b> to Whenever possible or Always.			
Prerequisites	cgsl_0	205:Signal handling for multirate models on page 3-12			
Rationale	A,B, C,D	Following this guideline protects data against possible corruption of preemptive (interruptible) operating systems.			
Note		asking systems with a non-preemptive operating system do not require data ity or determinism protection. In this case, clear these parameters:			
	Rate Transition block parameter Ensure data integrity during data transfer				
	Configuration parameter Ensure deterministic data transfer (maximum delay)				
	Ensuring data integrity and determinism requires additional memory and execution time. To reduce this additional expense, evaluate signals to determine the level of protection that they require.				
See Also	• Rat	te Transition			
	• "Da	ata Transfer Problems" (Simulink Coder)			
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### **Configuration Parameter Considerations**

- "cgsl\_0301: Prioritization of code generation objectives for code efficiency" on page 4-2
- "cgsl 0302: Diagnostic settings for multirate and multitasking models" on page 4-3

### cgsl\_0301: Prioritization of code generation objectives for code efficiency

ID: Title	cgsl_0301: Prioritization of code generation objectives for code efficiency			
Description	Prioritize code generation objectives for code efficiency by using the Code Generation Advisor.	n		
	A Assign priorities to code (ROM, RAM, and Execution efficiency) efficience objectives.	y		
	B Select the relative order of ROM, RAM, and Execution efficiency based of application requirements.	n		
	C Configure the Code Generation Advisor to run before generating code by setting the <b>Check model before generating code</b> configuration parameter to On (proceed with warnings) or On (stop for warnings).			
Notes	A model's configuration parameters provide control over many aspects of generated code. The prioritization of objectives specifies how configuration parameters are set when conflicts between objectives occur.			
	Prioritizing code efficiency objectives above safety objectives may remove initialization or run-time protection code (for example, saturation range checking for signals out of representable range). Review the resulting parameter configurations to verify that safety requirements are met.			
Rationale	A, B, C When you use the Code Generation Advisor, configuration parameters confort to the objectives that you want and they are consistently enforced.	rm		
See also	"Application Objectives Using Code Generation Advisor" (Simulink Coder)			
	"Manage Configuration Sets for a Model"			
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# cgsl\_0302: Diagnostic settings for multirate and multitasking models

ID: Title	cgsl_0302: Diagnostic settings for multirate and multitasking models
Description	For multirate models using either <b>single tasking</b> or <b>multitasking</b> , set these configuration parameters to warning or error:
	Single task rate transition
	Enforce sample time specified by Signal Specification blocks
	Detect multiple driving blocks executing at the same time step
	For <b>multitasking</b> models, set these configuration parameters to warning or error:
	Multitask task rate transition
	Multitask conditionally executed subsystem
	Tasks with equal priority
	If the model contains Data Store Memory blocks, set these configuration parameters to Enable all as warnings or Enable all as errors:
	Detect read before write
	Detect write after read
	Detect write after write
	Multitask data store
Rationale	Setting diagnostic configuration parameters improves run-time detection of rate and tasking errors.
See Also	"Model Configuration Parameters: Diagnostics"
	"hisl_0013: Usage of data store blocks"
	• "hisl_0044: Configuration Parameters > Diagnostics > Sample Time"
	• "hisl_0303: Configuration Parameters > Diagnostics > Data Validity > Merge blocks"
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